查询SY100E171供应商

3-BIT 4:1 MULTIPLEXER

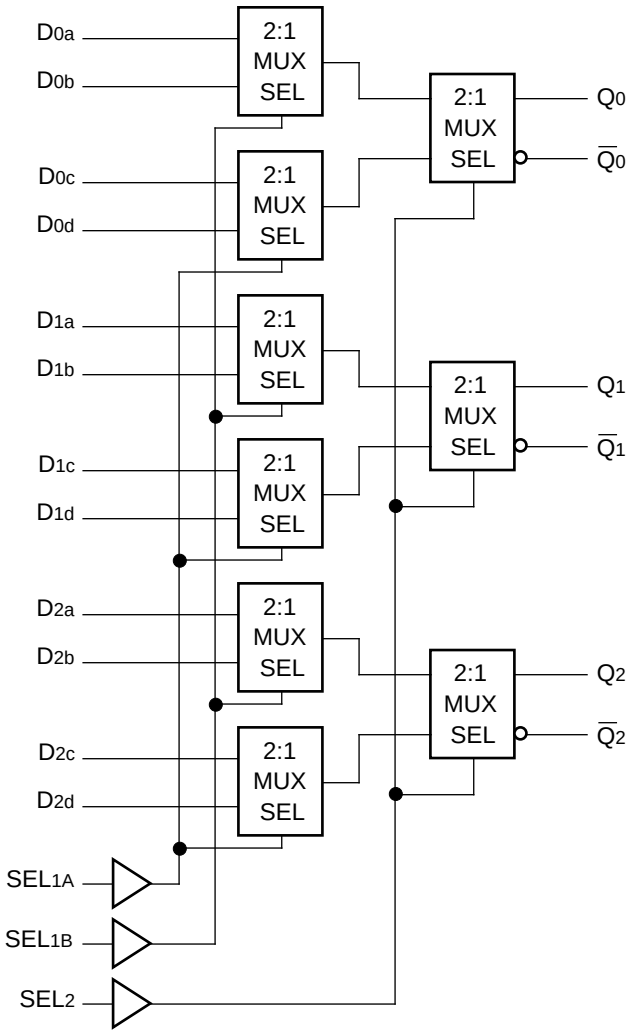
FEATURES

- **725ps max. D to output**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **Differential outputs**
- **Split select architecture**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E171**
- **Available in 28-pin PLCC package**

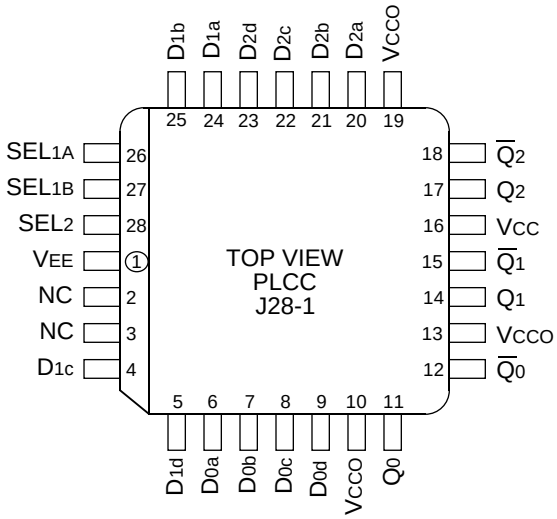
DESCRIPTION

The SY10/100E171 offer three 4:1 multiplexers with differential outputs, designed for use in new, high-performance ECL systems. The leading 4-bit multiplexer operation is organized pairwise, with each pair being a 2-bit multiplexer. Separate select (SEL_{1A}, SEL_{1B}) controls are provided within each pair. The SEL_{1A} and SEL_{1B} signals control the leading multiplexers, while the SEL_2 signal controls the output multiplexer. The three select signals can be used to determine which of the four data inputs will be propagated to the corresponding outputs.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_{0x}–D_{2x}	Data Inputs
SEL_{1A}, SEL_{1B}	First-stage Select Inputs
SEL_2	Second-stage Select Input
Q_0–Q_2	True Output
$\overline{Q}_0$–$\overline{Q}_2$	Inverted Output
V_{CCO}	V_{CC} to Output

Rev.: C Amendment: /1
Issue Date: February, 1998

TRUTH TABLE

Pin	State	Operation
SEL_2	H	Output c/d data
SEL_{1A}	H	Input d data
SEL_{1B}	H	Input b data

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	56	67	—	56	67	—	56	67		
	100E	—	56	67	—	56	67	—	65	77		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	275	480	650	275	480	650	275	480	650		
	SEL_1	450	650	850	450	650	850	450	650	850		
	SEL_2	350	550	700	350	550	700	350	550	700		
t_{skew}	Within-Device Skew										ps	1
	D_{nm}, D_{nm} to Q_n	—	60	—	—	60	—	—	60	—		
	D_a, D_b, D_c, D_d to Q	—	40	—	—	40	—	—	40	—		
t_r	Rise/Fall Time	300	475	650	300	475	650	300	475	650	ps	—
t_f	20% to 80%											

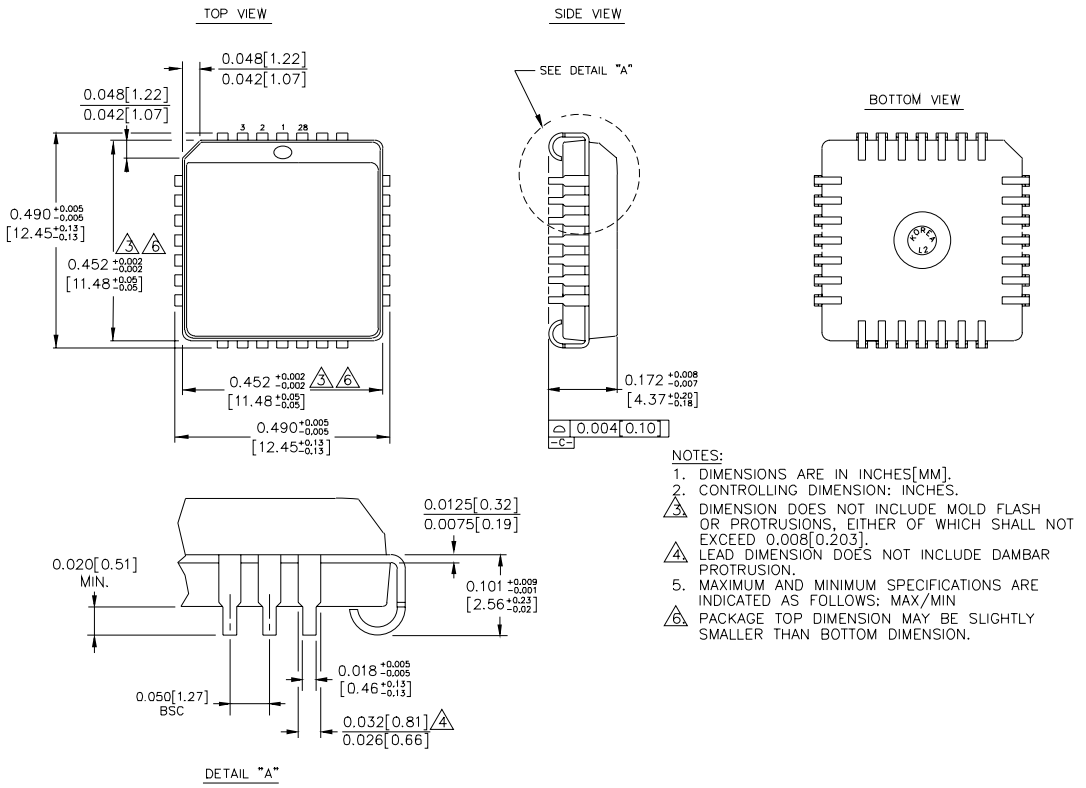
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device; n = 0, 1, 2 m = a, b, c, d.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E171JC	J28-1	Commercial
SY10E171JCTR	J28-1	Commercial
SY100E171JC	J28-1	Commercial
SY100E171JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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